THE INVENTION CLAIMED IS:

1. A method for manufacturing an image sensor comprising:
providing a substrate;
forming control circuitry on the substrate;
forming dielectric layers on the substrate;
forming interconnects in the dielectric layers in contact with the control circuitry;
forming pixel electrodes in contact with the interconnects;
forming an intrinsic layer (i-layer) over the pixel electrodes;
forming a gap in the i-layer between the pixel electrodes;
forming an i-layer covering layer over the i-layer; and
forming a transparent contact layer over the i-layer covering layer and the interconnects.

2. The method as claimed in claim 1 wherein:
forming the gap includes forming the i-layer into first and second i-layer portions.

3. The method as claimed in claim 1 including:
forming a pixel covering layer formed into first and second pixel covering layer portions over the pixel electrodes;
and wherein:
forming the gap includes forming the gap between the first and second pixel covering layer portions.

4. The method as claimed in claim 1 wherein:
forming the gap includes forming the i-layer covering layer into first and second i-layer covering layer portions.

5. The method as claimed in claim 1 wherein:
forming the i-layer covering layer wherein the i-layer covering layer is distal from the interconnects; and
forming the transparent contact layer wherein the transparent contact layer is in contact with the interconnects.

6. A method for manufacturing an image sensor comprising:

providing a semiconductor substrate;

forming pixel control circuitry on the substrate;

forming dielectric layers on the substrate;

forming interconnects in the dielectric layers in contact with the pixel control circuitry;

forming pixel electrodes in contact with the interconnects, the pixel electrodes of a material selected from a group consisting of a conductive semiconductor material and a conductive metal;

forming an intrinsic layer (i-layer) over the pixel electrodes;

forming a gap in the i-layer between the pixel electrodes;

forming a i-layer covering layer over the i-layer of a material selected from a group consisting of a p-doped material, an n-doped material, and a transparent conductive material; and

forming a transparent contact layer over the i-layer covering layer and the interconnects, the transparent contact layer of a material selected from a group consisting of a transparent conductive material.

7. The method as claimed in claim 6 wherein:

forming the gap includes forming the i-layer into first and second intrinsic layer portions.

8. The method as claimed in claim 6 including:

forming a pixel covering layer formed into first and second pixel covering layer portions over the pixel electrodes, the pixel covering layer of a material selected from a group consisting of an n-doped material and a p-doped material;

and wherein:

forming the gap includes forming the gap between the first and second pixel covering layer portions.

9. The method as claimed in claim 6 wherein:

forming the gap includes forming the i-layer covering layer into first and second i-layer covering layer portions.

10. The method as claimed in claim 6 wherein:

forming the i-layer covering layer wherein the i-layer covering layer is distal from the interconnects; and

forming the transparent contact layer wherein the transparent contact layer is over and in contact with the interconnects.

11. An image sensor comprising:

a substrate;

control circuitry on the substrate;

dielectric layers on the substrate;

interconnects in the dielectric layers in contact with the control circuitry;

pixel electrodes in contact with the interconnects;

an intrinsic layer (i-layer) over the pixel electrodes having a gap provided therein between the pixel electrodes;

an i-layer covering layer over the i-layer; and

a transparent contact layer over the i-layer covering layer and the interconnects.

12. The image sensor as claimed in claim 11 wherein:

the i-layer includes first and second i-layer portions separated by the gap.

13. The image sensor as claimed in claim 11 including:

a pixel covering layer formed over the pixel electrodes into first and second pixel covering layer portions separated by the gap.

14. The image sensor as claimed in claim 11 wherein:

the i-layer covering layer includes first and second i-layer covering layer portions separated by the gap.

15. The image sensor as claimed in claim 11 wherein:

the i-layer covering layer is distal from the interconnects; and

the transparent contact layer is in contact with the interconnects.

16. An image sensor comprising:

a semiconductor substrate;

pixel control circuitry on the substrate;

dielectric layers on the substrate;

interconnects in the dielectric layers in contact with the pixel control circuitry;

pixel electrodes in contact with the interconnects, the pixel electrodes of a material selected from a group consisting of a conductive semiconductor material and a conductive metal;

an intrinsic layer (i-layer) over the pixel electrodes and having a gap provided therein between the pixel electrodes;

a i-layer covering layer over the i-layer of a material selected from a group consisting of a p-doped material, an n-doped material, and a transparent conductive material; and

depositing a transparent contact layer over the second layer and the interconnects.

17. The image sensor as claimed in claim 16 wherein:

the i-layer includes first and second i-layer portions separated by the gap.

18. The image sensor as claimed in claim 16 including:

a pixel covering layer formed over the pixel electrodes into first and second pixel covering layer portions separated by the gap, the pixel covering layer of a material selected from a group consisting of an n-doped material and a p-doped material.

19. The image sensor as claimed in claim 16 wherein:

the i-layer covering layer includes first and second i-layer covering layer portions separated by the gap.

20. The image sensor as claimed in claim 16 wherein:

the i-layer covering layer is distal from the interconnects; and

the transparent contact layer is over and in contact with the interconnects.